In the Specification:

Please substitute the following paragraphs for the corresponding paragraphs for the corresponding numbered paragraphs in the specification as originally filed.

[0020] Figures 15A, 15B, 15C, 15D, 15E, 15F[[,]] and 15G ~~and 15H~~ illustrate application of the second embodiment of the invention to a top oxide late (TOL) process,

[0042] As shown in Figure 15E a layer of array top oxide is then deposited on the array and support areas. (Since the ATO is applied after formation of the gate polysilicon in the support area the process is referred to as top oxide late (TOL).) This results in a step height difference between the array and support areas approximately (e.g. due to the deep trench memory cell devices in the array area) equal to the thickness of the gate polysilicon which is relatively small in comparison with TOE processes. Therefore, further height equalization, as shown in Figure 15F is optional. If height equalization is performed, it is achieved by masking the array area with mask 161 and removing the ATO from the support area. This results in the topography of the array and support areas being of substantially equal height and step height, as shown in Figure 15F. Then, as shown in Figure 15G, ARC material is applied as described above and etching to or slightly into the surface of the memory cells 12 (preferably using end point detection) provides a planarized surface across both the array and support areas, as ~~shown in Figure 15H~~ discussed above with reference to Figures 13 and 14A.